

Dual P-Channel 60 V (D-S) MOSFET

| PRODUCT SUMMARY | | | |
|---------------------|------------------------------------|---------------------------------|-----------------------|
| V _{DS} (V) | R _{DS(on)} (Ω) | I _D (A) ^d | Q _g (Typ.) |
| - 60 | 0.055 at V _{GS} = - 10 V | - 6.2 | 23 nC |
| | 0.060 at V _{GS} = - 4.5 V | - 5.6 | |

FEATURES

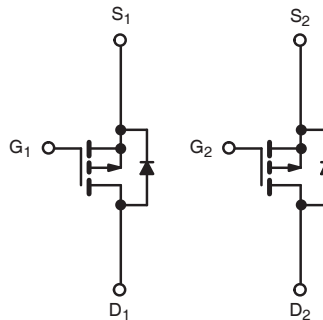
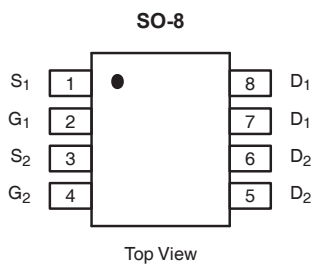
- DT-Trench Power MOSFET
- 100 % R_g and UIS Tested

APPLICATIONS

- Power management
- Load switch
- Battery protection



RoHS
COMPLIANT



P-Channel MOSFET P-Channel MOSFET

| ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted) | | | | |
|---|-----------------------------------|------------------------|-----------------------|---|
| Parameter | Symbol | Limit | Unit | |
| Drain-Source Voltage | V _{DS} | - 60 | V | |
| Gate-Source Voltage | V _{GS} | ± 20 | | |
| Continuous Drain Current (T _J = 150 °C) | I _D | T _C = 25 °C | -6.2 | A |
| | | T _C = 70 °C | -5.2 | |
| | | T _A = 25 °C | -2.7 ^{a,b} | |
| | | T _A = 70 °C | -1.3 ^{a,b} | |
| Pulsed Drain Current | I _{DM} | -24 ^e | | |
| Continuous Source-Drain Diode Current | I _S | T _C = 25 °C | - 6.2 | |
| | | T _A = 25 °C | - 2.5 ^{a, b} | |
| Avalanche Current | I _{AS} | -5.6 ^e | | |
| Single-Pulse Avalanche Energy | E _{AS} | 30 | mJ | |
| Maximum Power Dissipation | P _D | T _C = 25 °C | 10 | W |
| | | T _C = 70 °C | 7.1 | |
| | | T _A = 25 °C | 3.5 ^{a, b} | |
| | | T _A = 70 °C | 2.3 ^{a, b} | |
| Operating Junction and Storage Temperature Range | T _J , T _{stg} | - 55 to 175 | °C | |

| THERMAL RESISTANCE RATINGS | | | | |
|---|-------------------|---------|---------|------|
| Parameter | Symbol | Typical | Maximum | Unit |
| Maximum Junction-to-Ambient ^{a, c} | R _{thJA} | 23 | 40 | °C/W |
| Maximum Junction-to-Foot | R _{thJF} | 55 | 85 | |

Notes:

- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- Maximum under steady state conditions is 110 °C/W.
- Based on T_C = 25 °C.
- Limited by package.

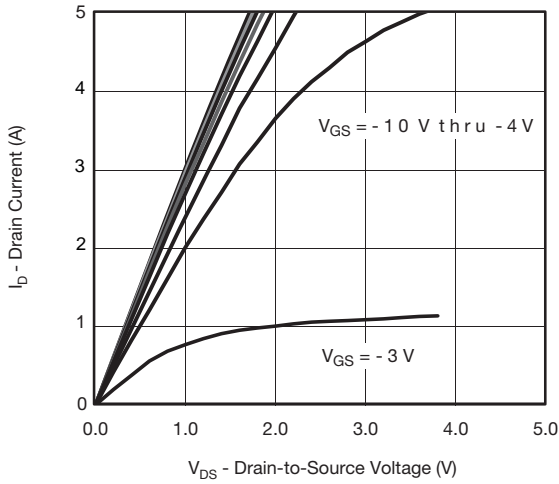
| SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted) | | | | | | |
|--|-------------------------|---|--------------------|-------|-----------|----------------------|
| Parameter | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
| Static | | | | | | |
| Drain-Source Breakdown Voltage | V_{DS} | $V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$ | - 60 | | | V |
| V_{DS} Temperature Coefficient | $\Delta V_{DS}/T_J$ | $I_D = -250\text{ }\mu\text{A}$ | | - 52 | | mV/ $^\circ\text{C}$ |
| $V_{GS(th)}$ Temperature Coefficient | $\Delta V_{GS(th)}/T_J$ | | | 4 | | |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$ | - 1 | | - 3 | V |
| Gate-Source Leakage | I_{GSS} | $V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$ | | | ± 100 | nA |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = -48\text{ V}, V_{GS} = 0\text{ V}$ | | | - 1 | μA |
| | | $V_{DS} = -48\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$ | | | - 10 | |
| On-State Drain Current ^a | $I_{D(on)}$ | $V_{DS} \geq -10\text{ V}, V_{GS} = -10\text{ V}$ | -7.9 | | | A |
| Drain-Source On-State Resistance ^a | $R_{DS(on)}$ | $V_{GS} = -10\text{ V}, I_D = -5\text{ A}$ | | 0.055 | 0.070 | Ω |
| | | $V_{GS} = -4.5\text{ V}, I_D = -4\text{ A}$ | | 0.060 | 0.075 | |
| Forward Transconductance ^a | g_{fs} | $V_{DS} = -15\text{ V}, I_D = -5\text{ A}$ | | 25 | | S |
| Dynamic^b | | | | | | |
| Input Capacitance | C_{iss} | $V_{DS} = -48\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$ | | 2475 | | μF |
| Output Capacitance | C_{oss} | | | 605 | | |
| Reverse Transfer Capacitance | C_{rss} | | | 53 | | |
| Total Gate Charge | Q_g | $V_{DS} = -48\text{ V}, V_{GS} = -10\text{ V}, I_D = -5\text{ A}$ | | 23 | 42 | nC |
| | | $V_{DS} = -48\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -4\text{ A}$ | | 18 | | |
| Gate-Source Charge | Q_{gs} | $V_{DS} = -48\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -4\text{ A}$ | | 5 | | nC |
| Gate-Drain Charge | Q_{gd} | | | 6 | | |
| Gate Resistance | R_g | | $f = 1\text{ MHz}$ | | 8 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD} = -48\text{ V}, R_L = 2\text{ }\Omega$ $I_D \cong -2\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\text{ }\Omega$ | | 10 | | ns |
| Rise Time | t_r | | | 9 | | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 60 | | |
| Fall Time | t_f | | | 25 | | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD} = -48\text{ V}, R_L = 2\text{ }\Omega$ $I_D \cong -1\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\text{ }\Omega$ | | 19 | | ns |
| Rise Time | t_r | | | 15 | | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 75 | | |
| Fall Time | t_f | | | 30 | | |
| Drain-Source Body Diode Characteristics | | | | | | |
| Continuous Source-Drain Diode Current | I_S | $T_C = 25\text{ }^\circ\text{C}$ | | | - 6.2 | A |
| Pulse Diode Forward Current | I_{SM} | | | | - 24 | |
| Body Diode Voltage | V_{SD} | $I_S = -2\text{ A}, V_{GS} = 0\text{ V}$ | | - 0.7 | - 1.2 | V |
| Body Diode Reverse Recovery Time | t_{rr} | $I_F = -2\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$ | | 25 | 52 | ns |
| Body Diode Reverse Recovery Charge | Q_{rr} | | | 22 | 61 | nC |
| Reverse Recovery Fall Time | t_a | | | 10 | | ns |
| Reverse Recovery Rise Time | t_b | | | 15 | | |

Notes:

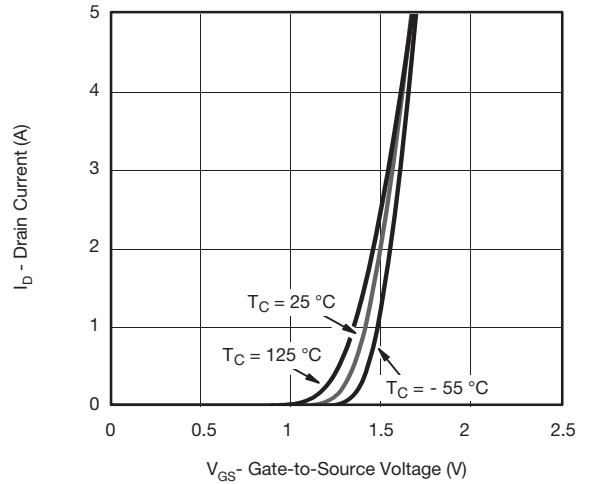
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

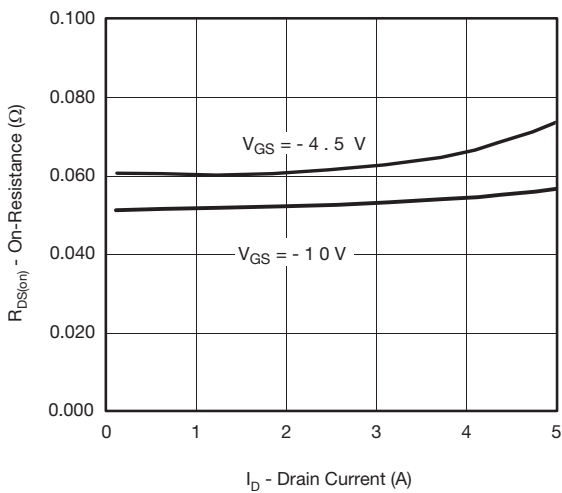
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



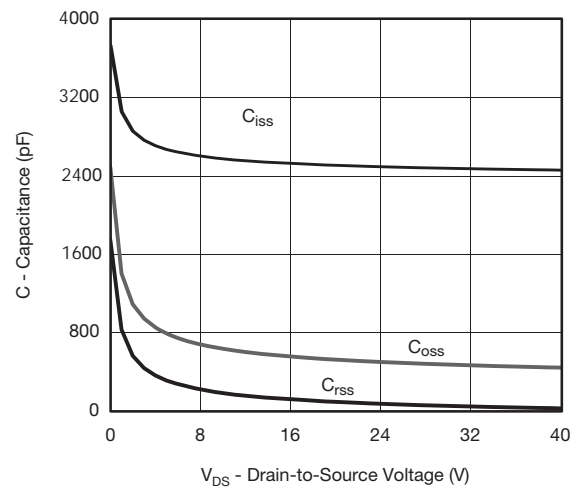
Output Characteristics



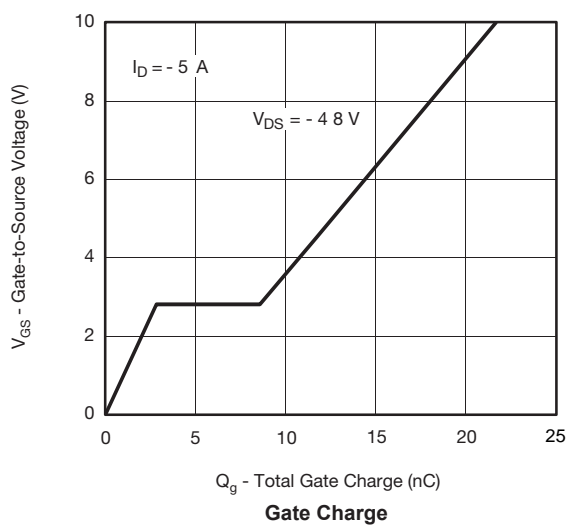
Transfer Characteristics



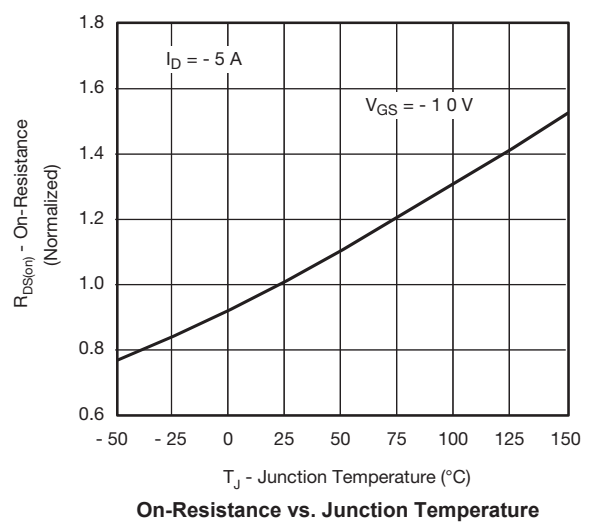
On-Resistance vs. Drain Current



Capacitance

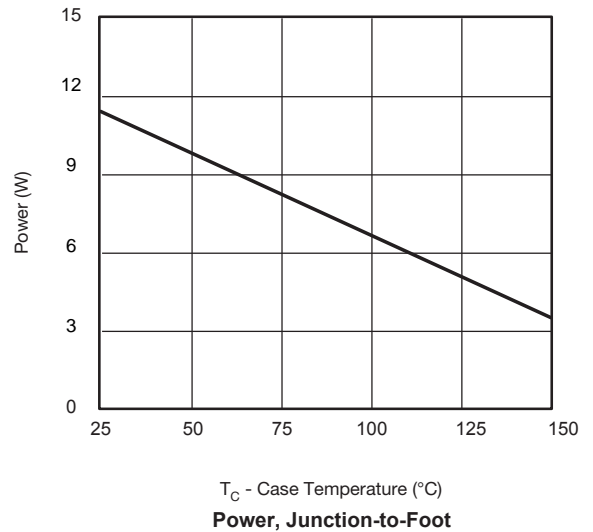
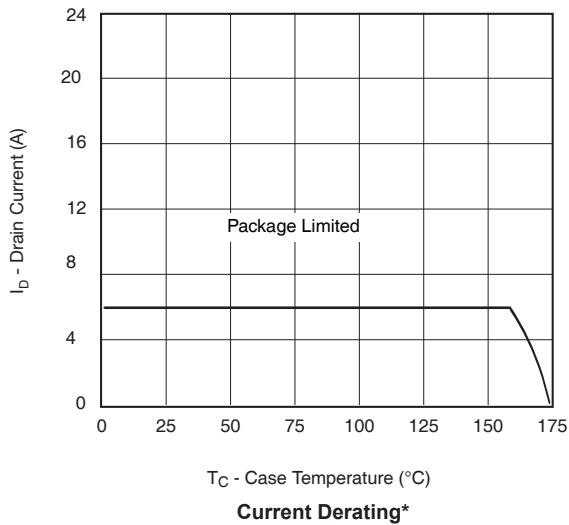
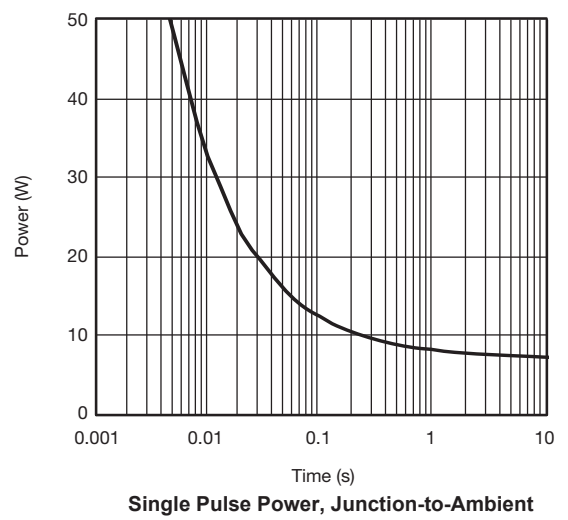
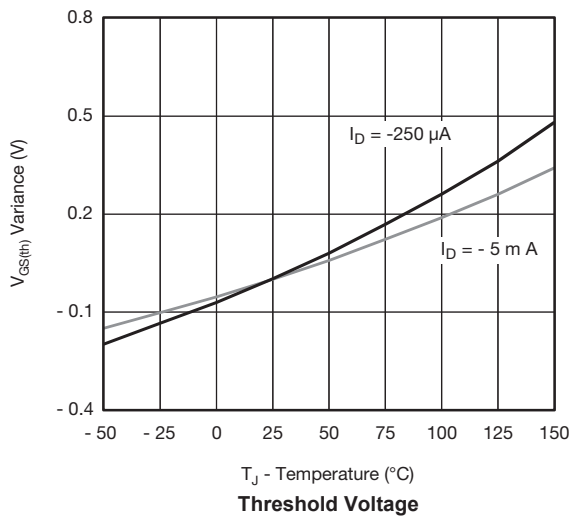
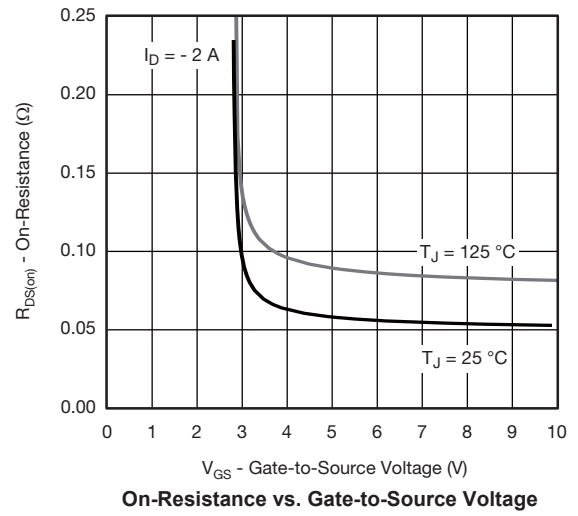
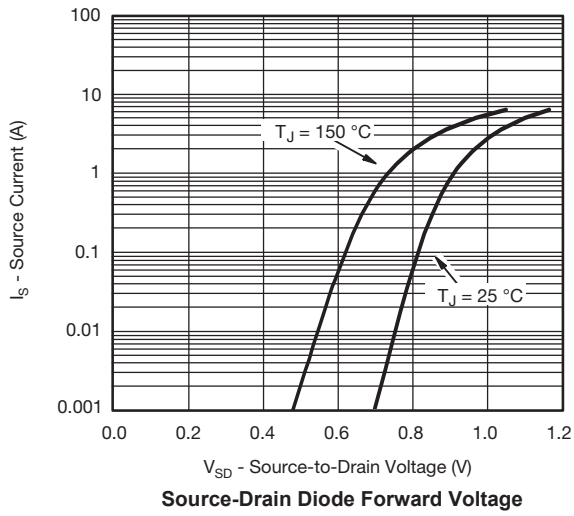


Gate Charge

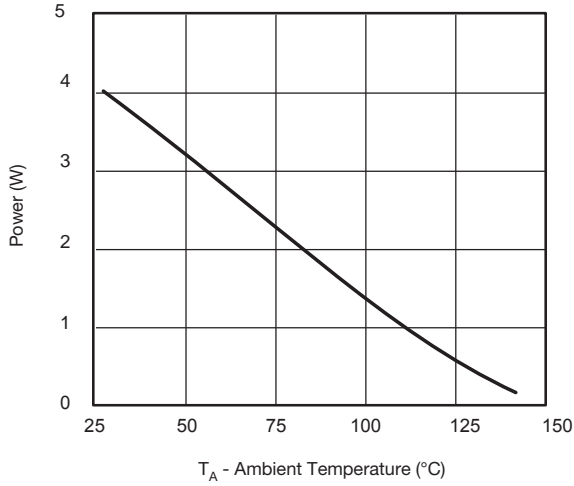


On-Resistance vs. Junction Temperature

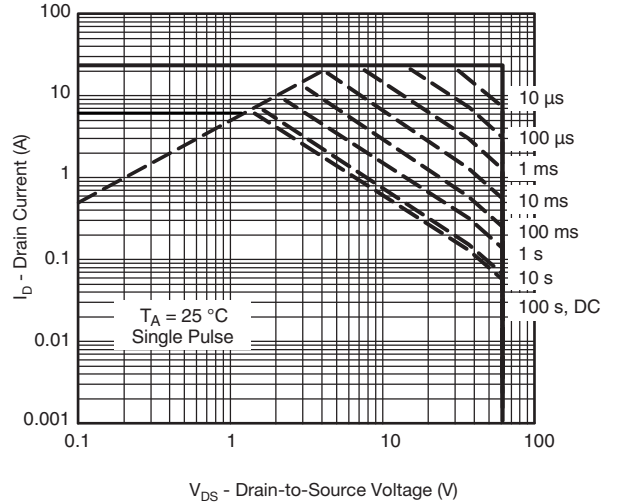
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



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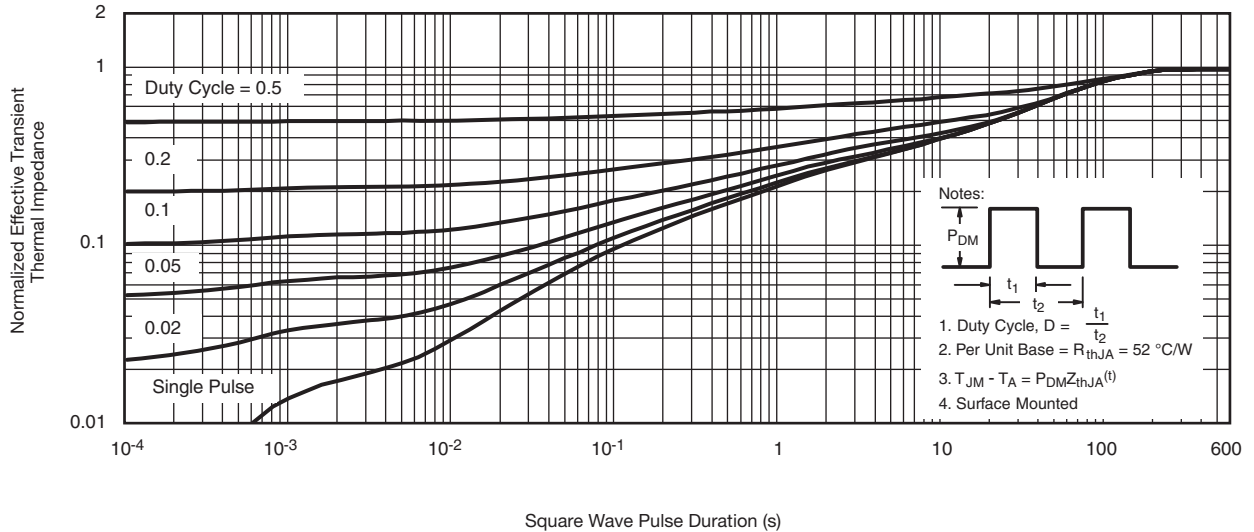


Power Derating, Junction-to-Ambient



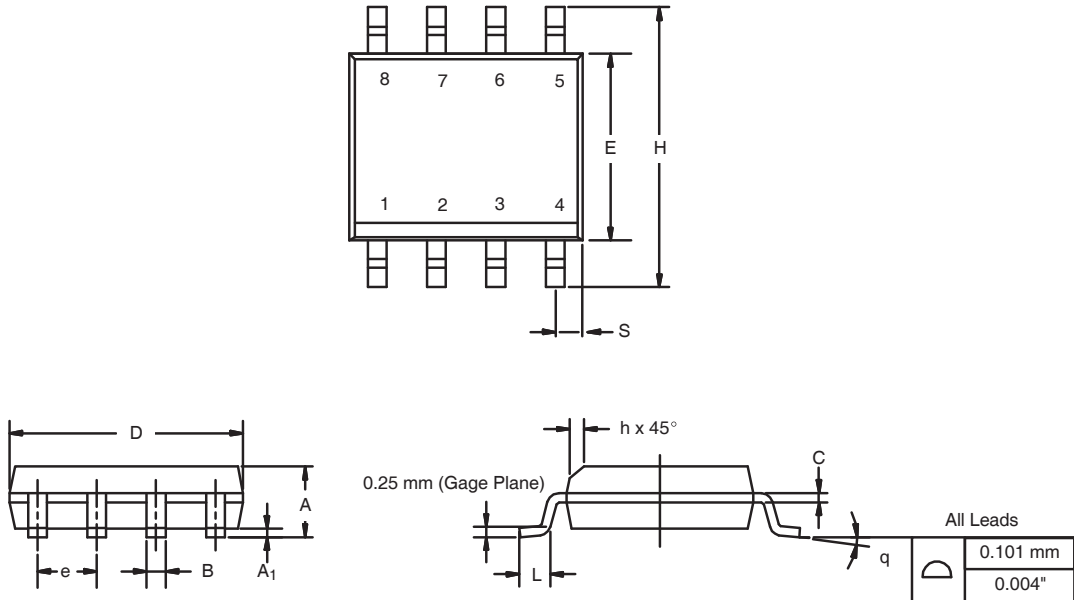
Safe Operating Area
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

* The power dissipation P_D is based on $T_{J(max)} = 150\text{ °C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



Normalized Thermal Transient Impedance, Junction-to-Ambient

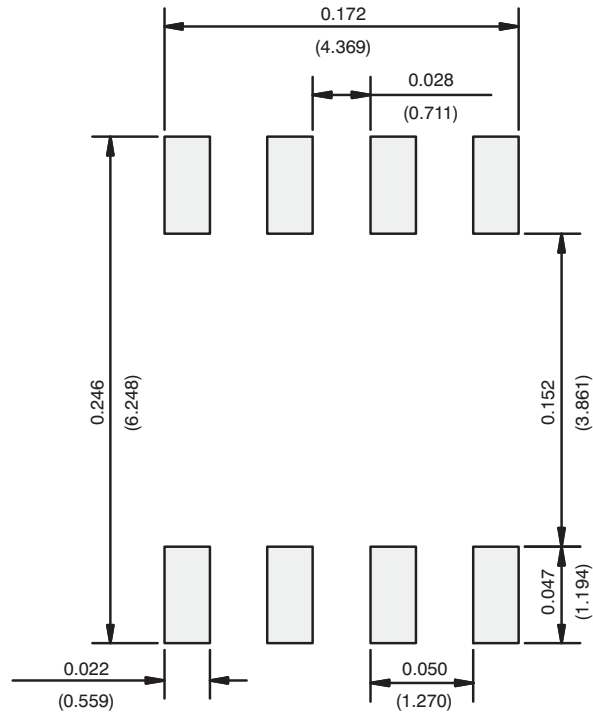
SOIC (NARROW): 8-LEAD
JEDEC Part Number: MS-012



| DIM | MILLIMETERS | | INCHES | |
|----------------|-------------|------|-----------|-------|
| | Min | Max | Min | Max |
| A | 1.35 | 1.75 | 0.053 | 0.069 |
| A ₁ | 0.10 | 0.20 | 0.004 | 0.008 |
| B | 0.35 | 0.51 | 0.014 | 0.020 |
| C | 0.19 | 0.25 | 0.0075 | 0.010 |
| D | 4.80 | 5.00 | 0.189 | 0.196 |
| E | 3.80 | 4.00 | 0.150 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| h | 0.25 | 0.50 | 0.010 | 0.020 |
| L | 0.50 | 0.93 | 0.020 | 0.037 |
| q | 0° | 8° | 0° | 8° |
| S | 0.44 | 0.64 | 0.018 | 0.026 |

ECN: C-06527-Rev. I, 11-Sep-06
DWG: 5498

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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